**WEEK3 PROGRAM 1**

**16 BIT ALU Simulation**

**Students have to complete the alu.v file**

Step1) **iverilog -o testalu lib.v alu.v tb\_alu.v**

If the compilation went OK, you won't see any output. What this does is create a file called testfa that we can feed to the simulator.

Step2) **vvp testalu**

You can observe output on the console

Step3) **gtkwave tb\_alu.vcd**

Output waveform will be observed.